DATA SHEET

BSN20
N-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of April 1995
File under Discrete Semiconductors, SC13b

1997 Jun 18

Philips Semiconductors

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N-channel enhancement mode vertical D-MOS transistor

BSN20

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- General purpose fast switching applications.

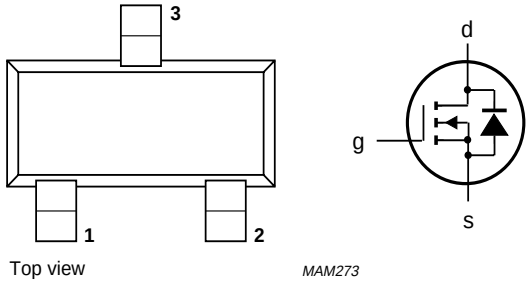
DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Marking code: M8p.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		50	V
I_D	drain current (DC)		100	mA
R_{DSon}	drain-source on-state resistance	I_D = 100 mA; V_{GS} = 10 V	15	Ω
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	1.8	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	300	mW
		up to T_{amb} = 25 °C; note 2	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	430	K/W
		note 2	500	K/W

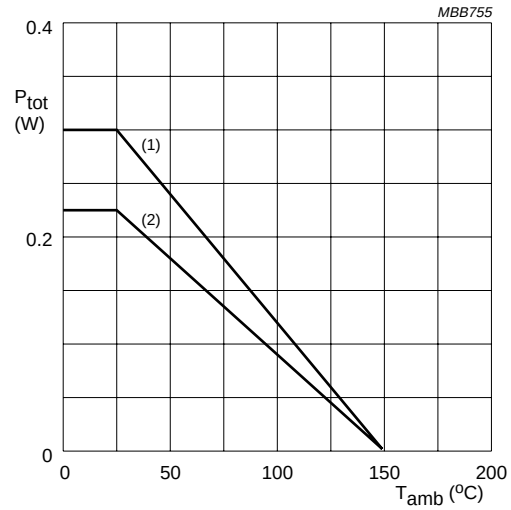
Notes to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate, $10 \times 8 \times 0.7$ mm.
2. Device mounted on a printed-circuit board.

CHARACTERISTICS

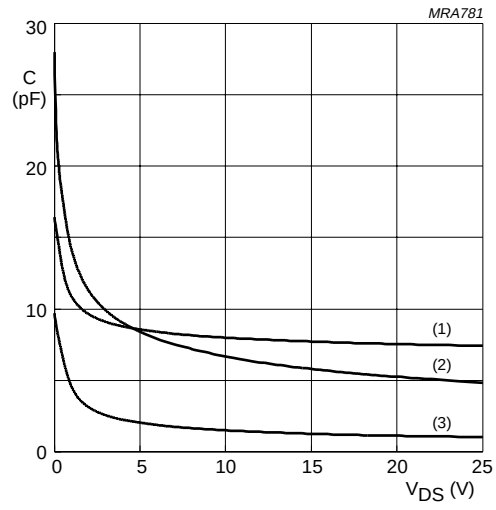
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	1.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 40 V	–	–	1	μA
I_{GSS}	gate-source leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 100 mA	–	8	15	Ω
		V_{GS} = 5 V; I_D = 100 mA	–	14	20	Ω
		V_{GS} = 2.5 V; I_D = 10 mA	–	18	30	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 10 V; I_D = 100 mA	40	80	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	7	15	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 100 mA	–	2	5	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 100 mA	–	5	10	ns



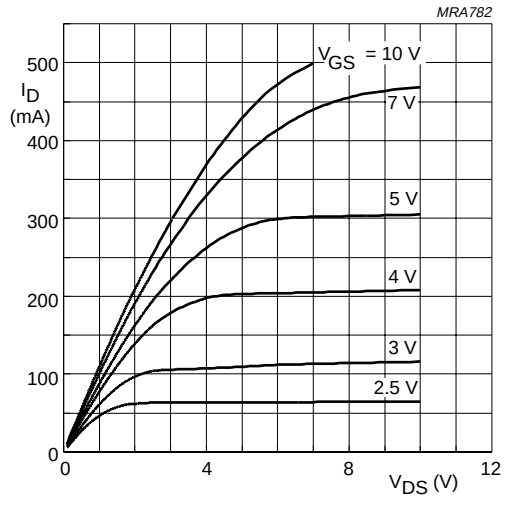
(1) Mounted on a ceramic substrate.
(2) Mounted on a printed-circuit board.

Fig.2 Power derating curves.



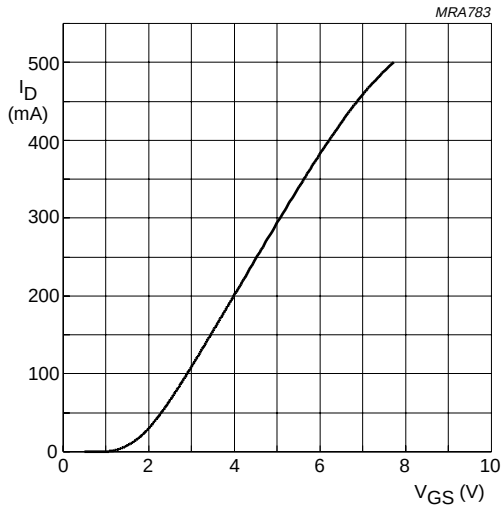
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.
(1) C_{is}.
(2) C_{os}.
(3) C_{rs}.

Fig.3 Capacitance as a function of drain source voltage; typical values.



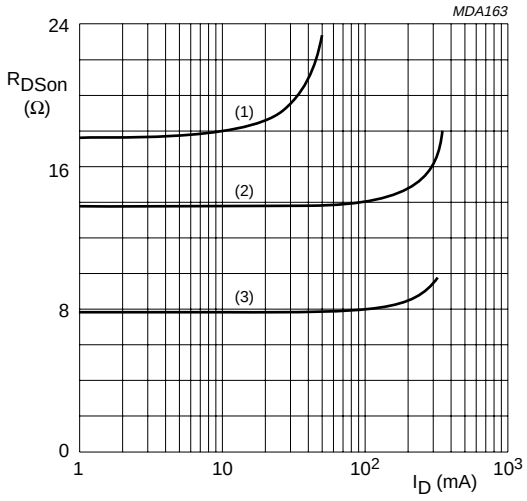
T_j = 25 °C.

Fig.4 Typical output characteristics.



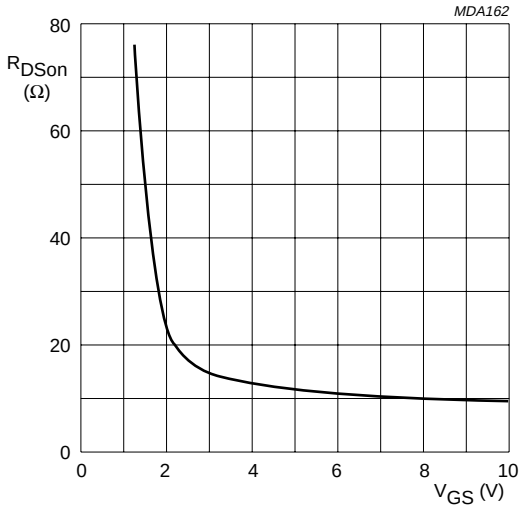
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



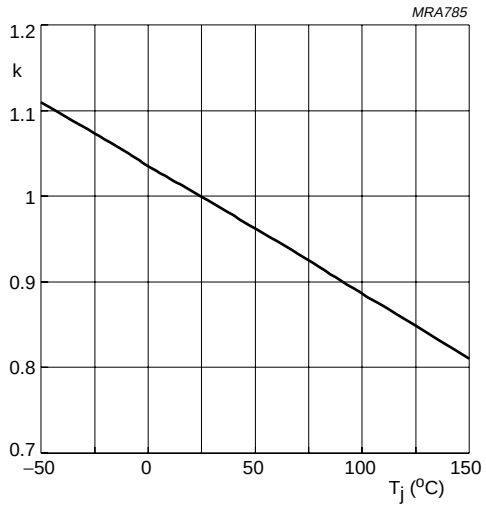
T_j = 25 °C.
(1) V_{GS} = 2.5 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of drain current; typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

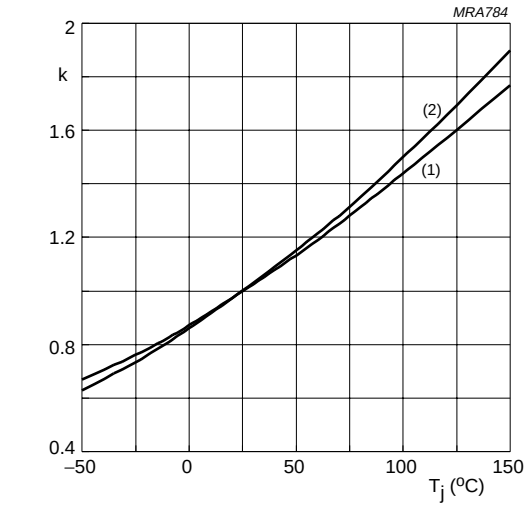
Fig.7 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at 1 mA.

Fig.8 Temperature coefficient of gate-source threshold voltage.



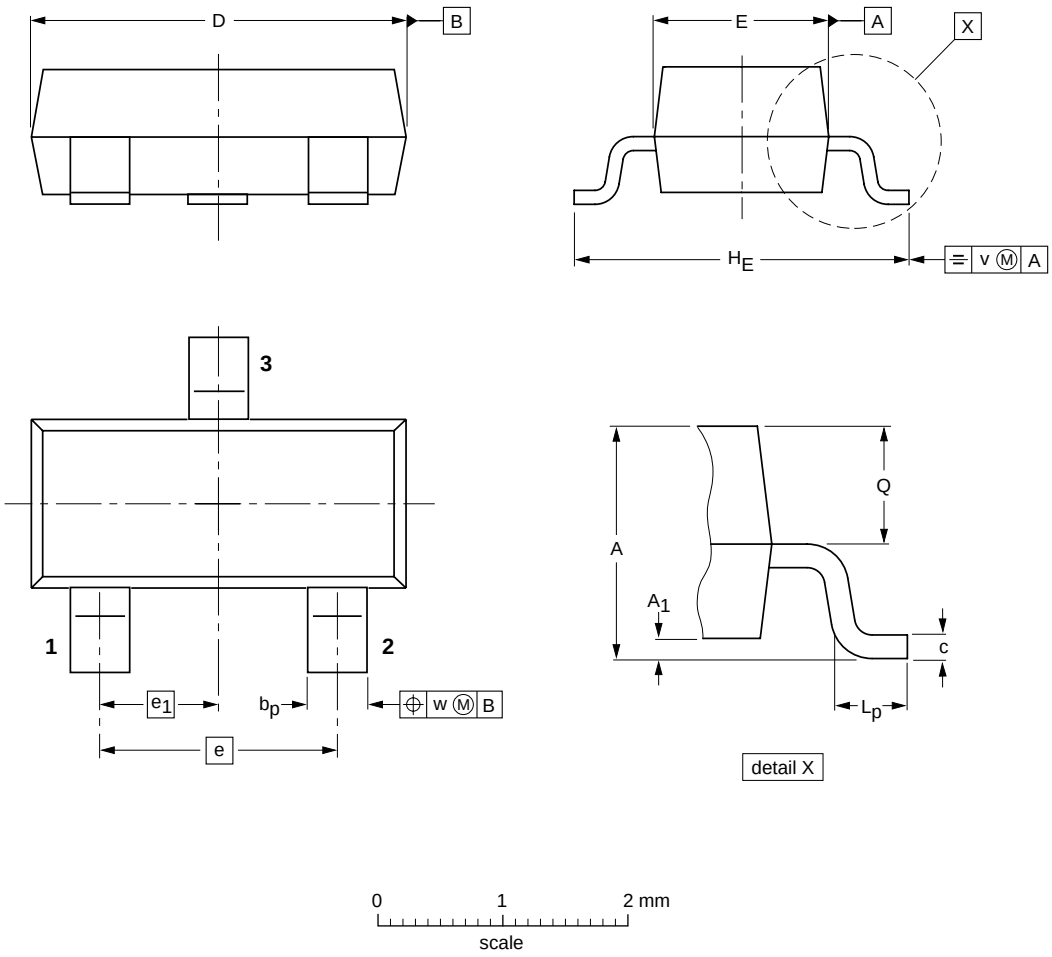
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) I_D = 10 mA; V_{GS} = 2.5 V.
(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.9 Temperature coefficient of drain-source on-state resistance.

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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